

Cyan Systems CS-4

1920 (H) x 1080 (V)

2.1 Mpixel Digital Readout Integrated Circuit

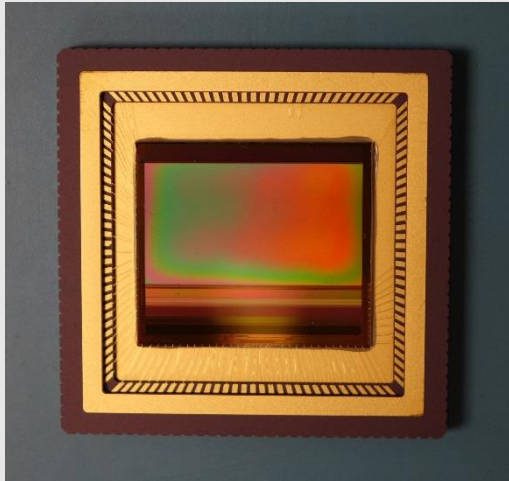


Figure 1. CS-4 Readout Integrated Circuit

Key Features

- 2.1M active unit cells (1920 H x 1080 V)
- Unit cell pitch (12 μm)
- Direct Injection unit cell preamplifier
- Accommodation for large detector bias
- P-on-N or N-on-P detector bias compatible
- Detector short-circuit protection
- Unit cell over-voltage clamping
- Effective noise suppression
- Advanced features, e.g. digital cal., BPR
- Automatic in-pixel background subtraction
- Full frame rate up to 120 Hz
- Programmable windowing operation
- SPI-based command & control interface
- Camera Link Base, Medium, 80b Full

Typical Applications

- ISR
- Security and surveillance
- Scientific imaging
- High speed imaging

Overview

High speed windowing HD 1080 digital readout integrated circuit (ROIC) simplifies system integration.

The CS-4 high speed windowing ROIC has a 1920 x 1080 format and 12 μm unit cell pitch.

The multiple-gain 2-color unit cell incorporates a direct injection (DI) preamplifier that can interface with P-on-N or N-on-P polarity C-QWIP or other detector arrays with large bias requirements. Detector short circuit protection and over-voltage clamping is designed into each unit cell.

The input circuit incorporates temporal sub-frame sampling providing effective noise suppression resulting in high quality imagery.

Column based analog-to-digital converters enable full format frame rate operation up to 120 Hz while programmable windowing enables frame rates into the kHz range based on window size and Camera Link output mode.

Other advanced features include nonlinearity correction, programmable gain, on-ROIC digital calibration and oversampling, pixel averaging, and bad pixel replacement.

Table 1. Key Performance Parameters

Parameter	Value
Resolution (full frame)	1920 (H) x 1080 (V)
Unit cell size (square)	12 μm
Optical size	23.0 mm x 13.0 mm
Unit cell preamplifier	Direct Injection
Detector type	P-on-N or N-on-P
Pixel gain states	4/2 (N-on-P/P-on-N)
Programmable col. gain	0.98 to 14.5
Programmable window sizes	30 x 1 (min) 1905 x 1079 (max) 15 x 1 resolution
Noise (low/high flux) ¹	400/1600 μV 2.1/8.5 counts PRELIMINARY
Readout modes	Snapshot ITR or IWR Frame-on-demand Free-run
Frame rate (full frame) (30 x 1 window)	0-120 Hz >10 kHz (min)
Clocks	1 (min)
Biases	9 (max)
Input clock freq. (LVDS)	70-297.5 MHz PRELIMINARY
Video outputs (LVDS)	5, 10, or 15 pair
Serial video clock rate	20-85 MHz
Camera Link modes	16-20 bit Base, 1 tap 16 bit Med., 3 tap 16 bit Ext. Full, 5 tap
Detector bias range	-16.5 to 3 V
Supply voltages	0 to 3.45V
Power (full frame, typ.) 30/60/120 Hz	150/250/325 mW MODE DEPENDENT PRELIMINARY
Operating temperature	≥ 55 K

Notes:

1. 80 K, SFA on, low flux = $1\text{E}14$ ph/cm²s
High flux = $1\text{E}18$ ph/cm²s



Signals, Biases, and IO

Many key biases and clock signals used for external control are made available to support various detector requirements, e.g. fine-tuned reverse bias, clock noise feed-through optimization, and variable integration. Only a single LVDS input clock is required in addition to 4-5 unique bias levels for typical operation. LVDS outputs conform to the Camera Link standard for Base, Medium, and 80b Full modes using 1, 3, and 5 taps, respectively.

Command Interface

Command and control of the CS-4 ROIC is performed using a proprietary Serial Peripheral Interface (SPI) based protocol. Cyan Systems uses a standard MOSI/MISO serial timing scheme integrated with the clocks that works with popular drive electronics and test sets.

Leadless Chip Carrier Wiring Diagram

Wiring diagrams for ROIC-to-COTS or custom leadless chip carriers (LCC) will be provided.

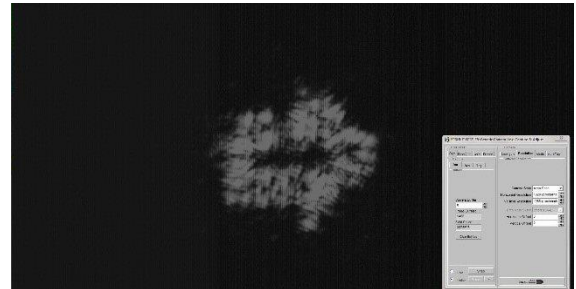


Figure 2. Uncorrected image of visible response to incident penlight on the CS-4 readout integrated circuit

For Additional Information

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