Cyan Systems CS-2

320 (H) x 256 (V)

Motion Computation Readout Integrated Circuit

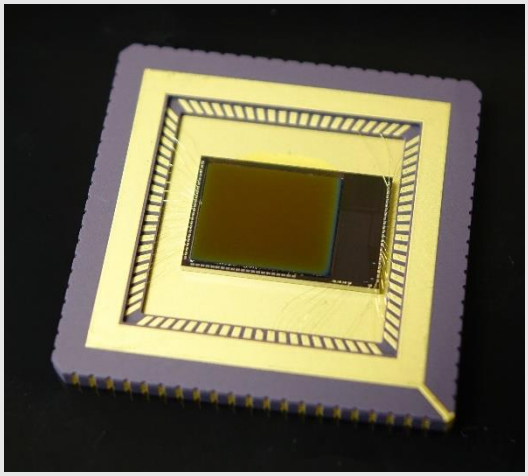

Figure 1. CS-3 Readout Integrated Circuit

Key Features

- 81,920 active unit cells (320 H x 256 V)
- Multiple detector type compatibility
- Suitable for high leakage detectors
- Accommodation for large detector bias
- CTIA unit cell preamplifier
- Dark current noise suppression
- Spatial processing
- On-ROIC motion computation
- Snapshot variable time integration
- 320 x 256 frame rate up to 60 Hz
- 32 x 32 tiled frame rate up to 3.1 kHz
- I^2C-bus command interface

Typical Applications

- Surveillance
- Scientific imaging
- Tracking moving objects

Overview

Advanced high frame rate motion computation readout integrated circuit (ROIC) operates in multiple modes.

Cyan Systems' advanced motion computation ROIC has a 320 x 256 format and 30 µm unit cell pitch.

The unit cell based capacitive transimpedance amplifier (CTIA) enables the use of nearly all type III-V and II-VI P-on-N polarity detector arrays with impedances typical of SWIR, MWIR, and LWIR. The ROIC supports detectors with a wide range of impedances and operating temperatures as a result of flexible leakage current tolerance, and lower de-biasing effects.

The unit cell incorporates dark current noise suppression. This enables the reduction of excess dark current noise often associated with developmental detector arrays resulting in higher quality imagery.

Additionally, the ROIC accommodates modern detectors with large bias requirements.

The ROIC supports multiple operating modes including standard video, noise averaging, motion computation, and spatial processing. The motion computation enables tracking of moving objects by outputting full resolution or a binary image at tiled frame rates up to 3.1 kHz. See Figures 2 and 3.

Table 1. Key Performance Parameters

Parameter	Value
Resolution (full frame)	320 (H) x 256 (V)
Unit cell size (square)	30 µm
Optical size	9.6 mm x 7.7 mm
Unit cell preamplifier	CTIA
Detector type	P-on-N
Noise floor (high/low gain)	60 e- / 1000 e-
Frame rate (full/tiled)	60 Hz / 3.1 kHz
Data rate (per channel)	1.3 MHz (typ)
Clocks	Up to 15 (11 typ)
Biases	4 (min)
Output channels	
Analog	4
Digital	1
Readout modes	Full frame ITR Tiled (32x32) ITR
Input clock frequency	1.3 MHz
Supply voltages	
Analog	5.0-5.5 V
Digital	5.0-5.5 V
Output swing	0.2-3.5 V
Power (full frame/tiled)	TBD/TBD mW (typ)
Operating temperature	100-330 K (nom)

Notes: Mode defines number of clocks required
TEC package is typical to improve noise performance

Signals, Biases, and IO

Many key biases and clock signals used for external control are made available to support various detector requirements, e.g. high reverse bias, clock noise feed-through optimization, variable integration, and on-ROIC processing modes. Documentation is available to enable the user to perform built-in testing and diagnostics to facilitate their development and assist in their detector array demonstration.

Command Interface

Mode control of the CS-2 ROIC is performed using inter-integrated circuit (I^2C) bus interface, a multi-master, multi-slave, single-ended, serial computer bus standard.

Leadless Chip Carrier Wiring Diagram

Wiring diagrams for ROIC to COTS or ROIC to custom leadless chip carriers (LCC) can be provided.

Figure 1. SWIR day image of CS-3 ROIC hybridized to InGaAs detector material

Figure 2. SWIR night image of distant highway and airplane (left) and motion computation binary image (right) showing auto-detection of vehicles and airplane

For Additional Information

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